SoC Fabric IPs to Enable DVFS

Dolphin Integration

ABSTRACT

As battery powered applications become increasingly sophisticated with requirements for higher processing power, SoC designers have to design adopt advanced design techniques to maintain a low power consumption. Multiple power domains, multiple clock frequencies and multiple voltage levels are among these techniques to save energy, both in sleep and active modes. More advanced solutions, such as dynamic voltage and frequency scaling (DVFS) allow even better power savings through the adjustment of clock and voltage based on the workload requirements, in each SoC functional modes.

This presentation explains, through a concrete example in an advanced low-power TSMC process, how SoC designers may adopt design techniques as advanced as DVFS, without risks and at minimal extra design costs It describes an approach to identify the right trade-off between the DVFS settings to get the most energy efficiency circuit. The efficiency of a circuit is defined with MOPS/µW units to measure the impact of the computing power regarding the power consumption. It then illustrates how the use of Dolphin's innovative SoC Fabric IPs enable to implement in a single pass, the power regulation and of the activity control networks of an ultra-low power SoC, i.e. saving several months in the design cycle.

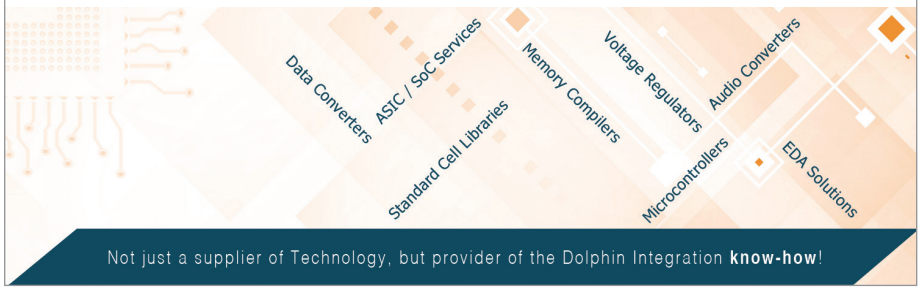
This presentation concludes on the next steps to enable Automatic Voltage and Frequency Scaling (AVFS) to maximize energy efficiency with a self-adjustment of voltage and frequency.

DOLPHIN INTEGRATION
The Enabler of Low-Power Systems-on-Chip

SoC Fabric IPs to Enable DVFS

LUCILLE ENGELS - OPERATION MANAGER FOR THE DESIGN AND THE SUPPLY OF CUSTOM ASICS

SEPTEMBER 2017 – SANTA CLARA



Not just a supplier of Technology, but provider of the Dolphin Integration **know-how**!

DOLPHIN INTEGRATION

SUMMARY

- IoT End Nodes challenges
- DVFS to reduce power consumption
- A concrete example with BLE Audio SmartHome
- SmartVision™, a SoC modeling platform for DVFS assessment
- FABRIC IPs for a straightforward implementation of DVFS
- A complete solution to enable DVFS

DOLPHIN INTEGRATION

IoT End Nodes Challenges

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DOLPHIN INTEGRATION

IoT END NODES CHALLENGES

Time To Market
- Reduce time to handle advanced low power design techniques
- Minimize efforts of sign-off verification
- Limit iterations costs between steps of design flow

Battery life time
- Anticipate power savings related to the use of advanced low power techniques
- Maximize the time spent in low consumption modes of each function
  - Operation at ultra Low Voltage capability
  - Selection of most power-efficient operating points
  - On-the-fly circuit operating points adaptation to its workload and environment (temperature, process, aging)

Reliability
- Manage local process variation
- Control aging phenomena
- Manage temperature variation

Connectivity
- Wireless connection
- Sensors/actuators network

Security
- Communication identification, encryption and integrity
- Detection and prevention of cyber attacks

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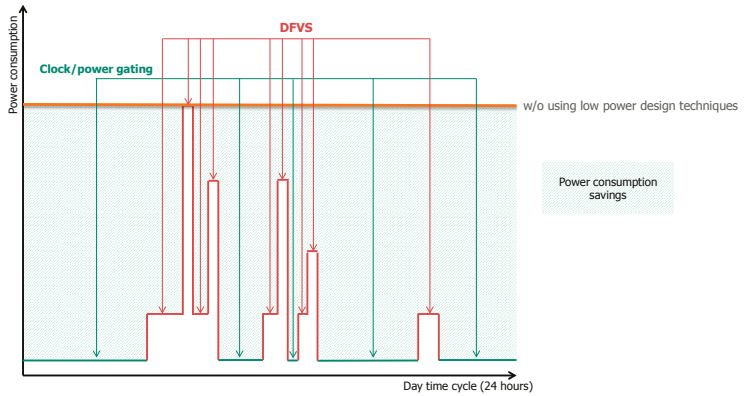
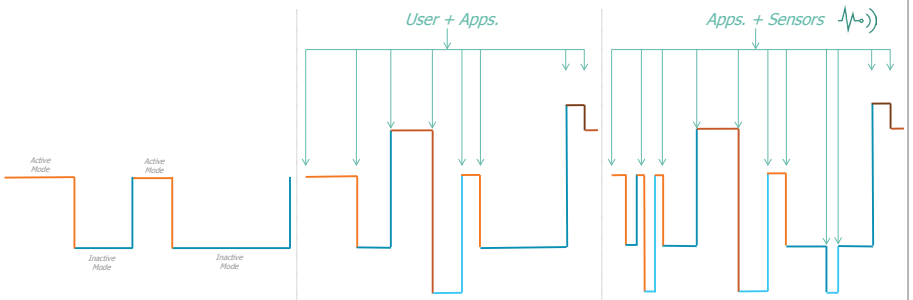
DVFS TECHNIC TO LOWER POWER CONSUMPTION

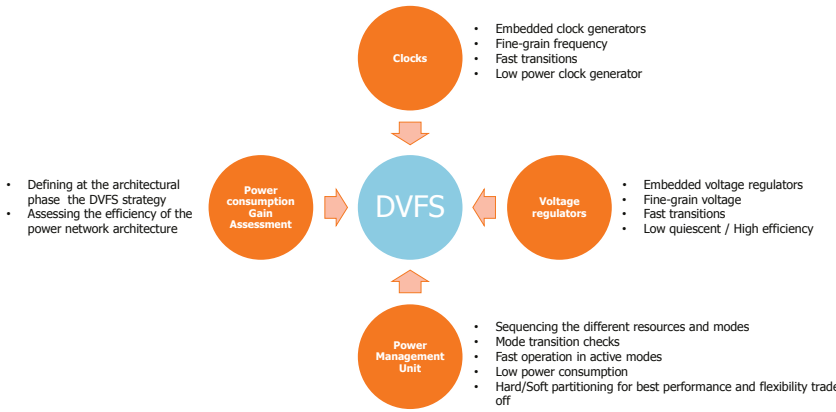


DVFS / AVFS TECHNIQUES DEFINITIONS



CLASSIC MODE CHANGES | DYNAMIC VOLTAGE FREQUENCY SCALING | ADAPTIVE VOLTAGE FREQUENCY SCALING

DESIGNING WITH DVFS IMPLIES



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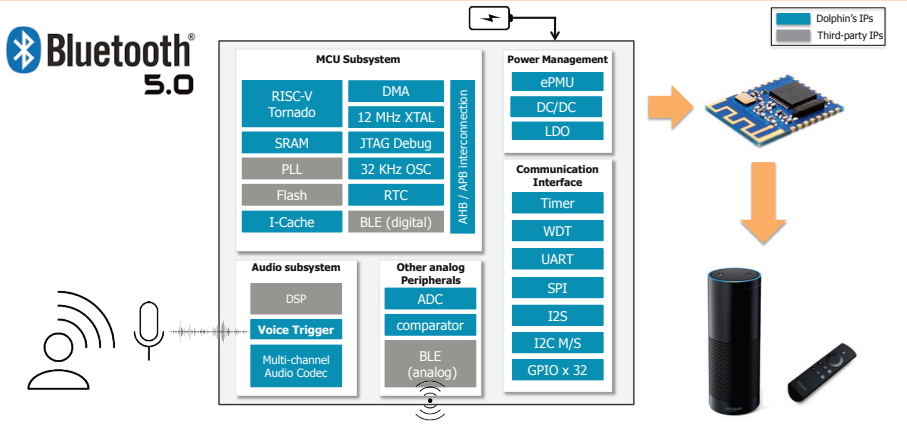
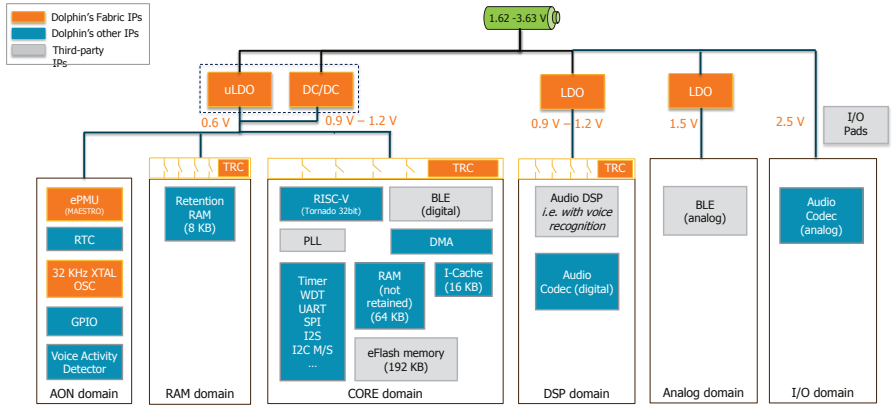
EXAMPLE OF BLE AUDIO SMARTHOME

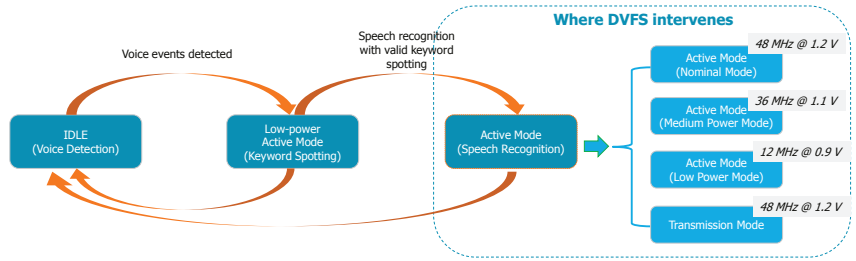


SOC POWER DOMAIN PARTITIONING

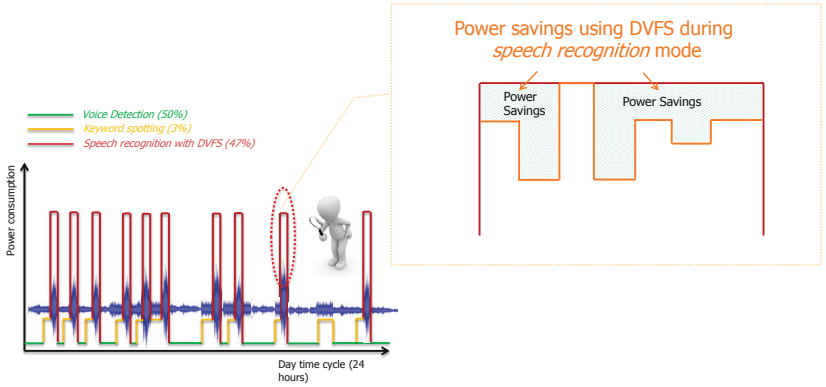


POWER MODE TABLE & MODE TRANSITIONS

Power Modes	IDLE / Standby (Voice Detection)	Low-power Active Mode (Keyword Spotting)	Active Mode (Speech Recognition)			
			Nominal Mode	*Medium Power Mode*	*Low Power Mode*	*Transmission Mode*
Time percentage on each mode	50%	3%	18%	16%	11%	2%
Power consumption target	< 50 µA @ 6 MHz 0.6 V	< 6 mA @ 12 MHz 0.9 V	< 32 mA @ 48 MHz 1.2 V	< 20 mA @ 36 MHz 1.1 V	< 8 mA @ 12 MHz 0.9 V	< 48 mA @ 48 MHz 1.2 V



LEVERAGING DVFS TO LOWER POWER CONSUMPTION



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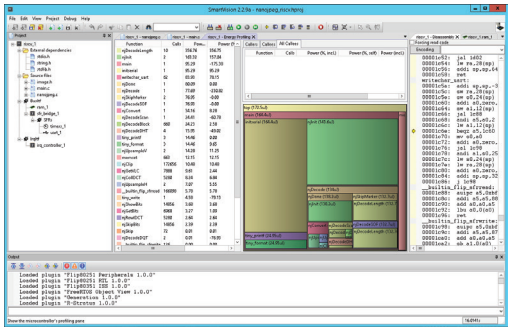
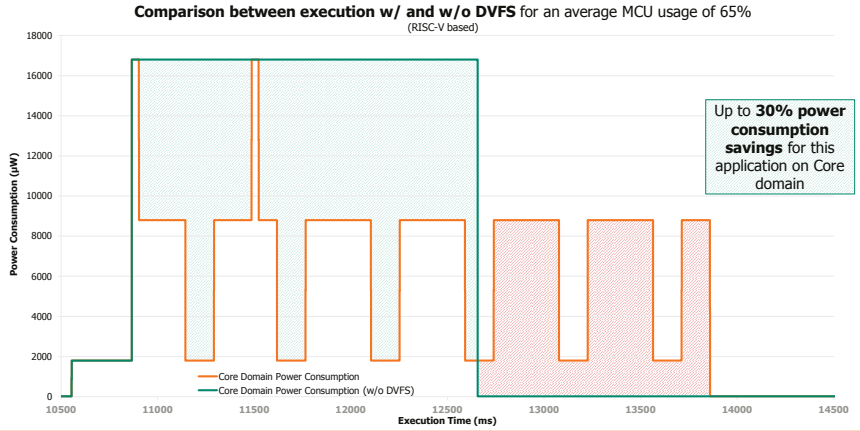
SMARTVISION™ SOC MODELING PLATFORM

Need to optimize the sub-system power consumption during software development and reduce Time-To-Market

- Need to take into account the complete subsystem with peripherals (power domains) and control network
  - Create and import models of components (RAM, analog blocks, etc.)
  - Group peripherals in power domains
  - Assess the impact of software coding on power consumption for each peripheral or for each power domain – to start software development faster and to debug it earlier
  - Manage through MAESTRO model the power management and transitions between modes
  - Simulate and verify mode transitions consistency (e.g. to detect the use by the software of a switched-off peripheral…)



SIMULATION RESULTS FOR BLE AUDIO SMARTHOME



REPORTS BASED ON SMARTVISION™

Power consumption reduction for an average of 65% of MCU usage (RISC-V based)

DVFS ON

	Always-On Domain	Core Domain	DSP Domain	RAM Domain	Analog Domain	I/O Domain	TOTAL
Power consumption (µW)	0.36	1804.95	79.65	900.89	470.07	784.73	**4040.65**

+ 2.9 % | - 30.5 % | +2.7 % | - 30.5 % | + 45.5 % | - 17.6 % | - 23 %

DVFS OFF (Nominal)

	Always-On Domain	Core Domain	DSP Domain	RAM Domain	Analog Domain	I/O Domain	TOTAL
Power consumption (µW)	0.35	2598.23	77.51	1295.00	323.13	952.37	**5246.59**

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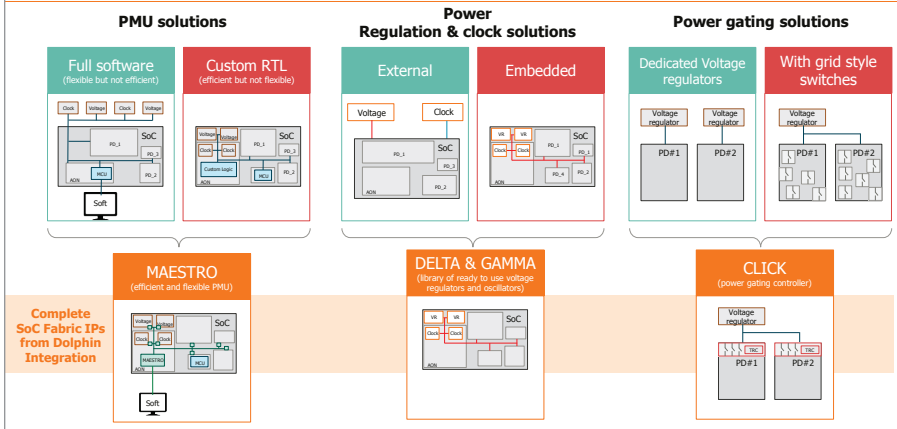
SOC FABRICS IPS: THE ENABLER OF DVFS



SOC FABRIC IPS TO ENABLE DVFS

FABRIC IPS FOR ULTRA LOW POWER SOCS

Activity Control Network
MAESTRO
- Reconfigurability
- Resource conflict management
- Boot-up sequence management
- Mode transition sequence management
- Native DVFS support

Power Regulation Network
DELTA
- Library of Voltage regulators
- Reusability
- Programmable output voltage
- Over-voltage operations

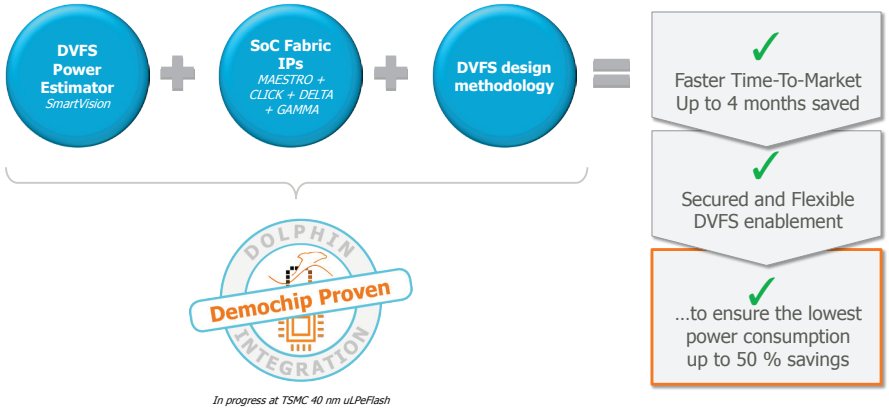
Power Gating Controller
CLICK
- Register programmable even after tape-out
- In-Rush current management
- Easy implementation
- Single-pass implementation

Clock Network
GAMMA
- Low Frequency
- Ultra Low power
- Fast wake up and high accuracy
- RC-based XTAL-based

FABRIC IPS FOR A FAST AND SAFE IMPLEMENTATION OF DVFS

Low Power PMNet	MAESTRO handles all the SoC power modes for **a safe, fast and efficient energy management** DELTA allows **different optimizations** of the power regulation network (PRNet) CLICK to **manage safely power gating** and save up to 99% on leakage current GAMMA for **ultra-low power oscillators**
Easy control of Voltage and clock	MAESTRO handles the **arbitration of the shared resource conflicts** MAESTRO + CLICK allow a **straightforward management of retention and shutdown** of island
Multi-frequency, multi-supply management	MAESTRO can either run with **slow clock** (32KHz) **for low power mode** or **fast system clock to speed up the transition** thus save further energy **Wide range of power modes** handled by Maestro **Fine-grain voltage adjustment** included in the DELTA library **Several characterizations** of the CLICK for a multi-supply architecture
Efficient power modes transitions	MAESTRO guarantees that the **voltage/clock transition can be performed in a secure way** CLICK **handles safely and automatically** the trade-off between wake-up time and in-rush current at block level DELTA incl. **fast voltage switching** regulators
Seamless SoC Integration	Fabric IPs ensures **a full inter-operability** **Silicon proven IPs** **Fully compliant** with conventional design flows and standard SoC busses

A COMPLETE SOLUTION TO ENABLE DVFS



In progress at TSMC 40 nm uLPeFlash

AVAILABILITY ON TSMC PROCESS

CLICK	DELTA	GAMMA	MAESTRO
• 55 nm LP, uLP, uLPeF; 180 nm eLL • In progress for 40 nm uLPeF & 28 nm HPC+	• From 180 nm down to 40 nm • In progress for 40 nm uLPeF & 28 nm HPC+	• 55 nm uLPeF • In progress for 40 nm uLPeF & 28 nm HPC+	• No process restriction